

WHAT IS CLAIMED IS:

1. A phase detector circuit that receives a random NRZ signal $V_i(t)$ having a period of T and a signal $V_i(t - \theta T/2\pi)$ having the same period and pattern as those of the signal $V_i(t)$ and delayed from the signal $V_i(t)$ by θ in phase, and outputs a signal including a DC voltage component associated with a phase difference θ between said two signals,

wherein an output $V_o(t)$ of the phase detector circuit is represented by:

$$V_o(t) = (V_i(t) - V_i(t-T)) \times V_i(t - \theta T / 2\pi),$$

where the signal $V_i(t-T)$ is delayed from the signal $V_i(t)$ by the period T of the signal $V_i(t)$.

2. A phase detector circuit that outputs a signal including a DC voltage component associated with a phase difference between two input signals, comprising:

a delay circuit for outputting a signal delayed by the time of T, which is a period of an input random NRZ signal;

a subtracter circuit for outputting a difference between said input random NRZ signal and the signal delayed by said delay circuit; and

a multiplier circuit for outputting a product of another input random NRZ signal having the same pattern as that of said input random NRZ signal and said phase difference and an output of said subtracter circuit.

3. A phase detector circuit that outputs a signal including a DC voltage component associated with a phase difference between two input signals, comprising:

a first multiplier circuit for outputting a product of an input random NRZ signal and another input random NRZ signal having the same pattern as that of the signal and said phase difference;

a delay circuit for outputting a signal delayed by the time of T , which is a period of said input random NRZ signal;

a second multiplier circuit, which is different from said first multiplier circuit, for outputting a product of said another input random NRZ signal and an output of said delay circuit; and

a subtracter circuit for outputting a difference between an output of said first multiplier circuit and an output of said second multiplier circuit.

4. A phase detector circuit that outputs a signal including a DC voltage component associated with a phase difference between two input signals, comprising:

a first voltage controlled delay circuit for outputting a delay applied to an input random NRZ signal by controlling the delay with a predetermined first signal;

a subtracter circuit for outputting a difference between an input random NRZ signal and a signal output from said first voltage controlled delay circuit;

a multiplier circuit for outputting a product of another input random NRZ signal having the same period and pattern as those of an input random NRZ signal and the phase difference and an output of said subtracter circuit; and

a control circuit for controlling said first voltage controlled delay circuit, the control circuit having:

an oscillator circuit for outputting a clock signal having the same period as the period T of an input random NRZ signal;

6. A phase detector circuit that outputs a signal including a DC voltage component associated with a phase difference between two input signals, comprising:

a delay circuit for outputting a signal delayed by the time of $(T-\delta T)$, which is a little shorter than the period T of an input random NRZ signal;

a subtracter circuit for outputting a difference between said input random NRZ signal and the signal delayed by said delay circuit;

a multiplier circuit for outputting a product of another input random NRZ signal having the same pattern as that of said input random NRZ signal and said phase difference and an output of said subtracter circuit.

7. A phase detector circuit that receives a random NRZ signal $V_i(t)$ having a period of T and a signal $V_i(t-\theta T/2\pi)$ having the same period and pattern as those of the signal $V_i(t)$ and delayed from the signal $V_i(t)$ by θ in phase, and outputs a signal including a DC voltage component associated with a phase difference θ between said two signals,

wherein an output $V_o(t)$ of the phase detector circuit is represented by:

$$V_o(t) = (V_i(t) - V_i(t - (T - \delta T))) \times V_i(t - \theta T/2\pi),$$

where the signal $V_i(t - (T - \delta T))$ is delayed from the signal $V_i(t)$ by the time of $(T - \delta T)$, which is a little shorter than the period T of the signal $V_i(t)$.

Added
a' 7